Amendments to the Claims

1. (Currently Amended) A self-testable double data rate (DDR) circuit, comprising:

a stimulus generator configured to generate a test DDR signal for testing an input/output interface of a DDR circuit;

an evaluator configured to compare said test DDR signal with a response signal produced by the input/output interface of the DDR circuit in response to said test DDR signal; and

a result generator configured to generate an error condition if said response signal does not have a predetermined relationship to said test DDR signal.

2. (Original) The self-testable DDR circuit of claim 1, wherein said stimulus generator, said evaluator and said result generator are located on a single semiconductor chip.

3. (Original) The self-testable DDR circuit of claim 2, wherein self-testing of said self-testable DDR circuit is performed without said test DDR signal or said response signal crossing a boundary of the semiconductor chip, thereby allowing said self-testing to be performed at an on-chip clock speed.

4. (Original) The self-testable DDR circuit of claim 1, wherein said stimulus generator comprises a linear feedback shift register.

5. (Original) The self-testable DDR circuit of claim 1, wherein said test DDR signal is generated and evaluated during a self-testing mode of operation controlled by a built-in self-test controller.

6. (Original) The self-testable DDR circuit of claim 5, wherein said response signal is produced by the DDR circuit at the same data rate as the DDR circuit operates during a normal mode of operation.

7. (Original) The self-testable DDR circuit of claim 1, wherein said evaluator is configured to perform said comparison dynamically as said response signal is generated.

8. (Original) The self-testable DDR circuit of claim 1, wherein said result generator is configured to maintain said error condition during generation and evaluation of a subsequent test DDR signal.

9. (Currently Amended) A double data rate (DDR) macro cell for a self-testable input/output interface, the macro cell comprising:

a signal generator configured to generate an input signal pattern for testing the input/output interface;

an evaluator configured to compare said input signal pattern with an output pattern produced by the input/output interface in response to said input signal pattern; and

a result generator configured to indicate an error if said output signal pattern differs from said input signal pattern;

wherein said signal generator, said evaluator and said result generator are located on a single semiconductor chip; and

wherein the input/output interface is an external interface configured to couple the single semiconductor chip to an external circuit.

10. (Original) The DDR macro cell of claim 9, wherein testing of the input/output interface is performed without said input signal pattern or said output signal pattern crossing a boundary of the semiconductor chip, thereby allowing said testing to be performed at an on-chip clock speed.

11. (Original) The DDR macro cell of claim 9, wherein said signal generator comprises a linear feedback shift register.

12. (Original) The DDR macro cell of claim 11, wherein said linear

feedback shift register has a characteristic polynomial of $x^{10} + x^3 + 1$.

13. (Original) The DDR macro cell of claim 9, wherein said evaluator performs said comparison in real-time as the input/output interface produces said output pattern.

14. (Original) The DDR macro cell of claim 9, wherein the input/output interface produces data in DDR form at a first data rate in a normal operating mode and produces said output pattern at said first data rate in a self-testing mode.

15. (Original) The DDR macro cell of claim 9, wherein the DDR macro cell is a DDR data output macro cell.

16. (Original) The DDR macro cell of claim 9, wherein the DDR macro cell is a DDR data input macro cell.

17. (Currently Amended) A double data rate (DDR) input/output interface of a first circuit, configured to couple the first circuit to an external circuit, the DDR input/output interface comprising:

a self-testable output macro cell;

a self-testable input macro cell; and

a self-testable clock macro cell;

wherein self-testing of said output macro cell, said input macro cell and said clock macro cell is performed entirely within the first circuit.

18. (Original) The DDR input/output interface of claim 17, further comprising a built-in self-test controller configured to control said self-testing of said output macro cell, said input macro cell and said clock macro cell.

19. (Original) The DDR input/output interface of claim 17, wherein said self-testing of each said macro cell is performed at an operational speed of said macro

cell.

20. (Original) The DDR input/output interface of claim 17, wherein one or more of said output macro cell and said input macro cell comprise:

a signal generator configured to generate a test signal for testing said macro cell;

an evaluator configured to compare said test signal with a response signal produced in response to said test signal; and

a result generator configured to indicate an error if said response signal differs from said test signal.

21. (Original) The DDR input/output interface of claim 20, wherein said signal generator, said evaluator and said result generator are located on a single semiconductor chip.

22. (Original) The DDR input/output interface of claim 21, wherein testing of said DDR input/output interface is performed without said test signal or said response signal crossing a boundary of the semiconductor chip, thereby allowing said testing to be performed at an on-chip clock speed.

23. (New) The self-testable DDR circuit of claim 1, wherein:

said self-testable DDR circuit is a single circuit; and

self-testing of said self-testable DDR circuit is performed without activating an external circuit.

24. (New) A double data rate (DDR) circuit for self-testing an external input/output interface of the circuit, the circuit comprising:

an input/output interface configured for coupling to an external circuit;

a set of DDR output macro cells;

a set of DDR input macro cells;

a set of clock macro cells;

a clock; and

a controller for controlling self-testing of the external input/output interface of the DDR circuit, using the DDR output macro cells, DDR input macro cells and clock macro cells, and without communicating with any external circuit.

25. (New) The DDR circuit of claim 24, wherein said DDR output macro cells comprise scan chain hookups to facilitate scanning.